100	**DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING**
1	.Reliability and availability
2	..Fault recovery
3	...By masking or reconfiguration
4	....Of network
5	....Of memory or peripheral subsystem
6	.....Redundant stored data accessed (e.g., duplicated data, error correction coded data, or other parity-type data)
7	......Reconfiguration (e.g., adding a replacement storage component)
8	.....Isolating failed storage location (e.g., sector remapping)
9	.....Access processor affected (e.g., I/O processor, MMU, DMA processor)
10	....Of processor
11	.....Concurrent, redundantly operating processors
12	......Synchronization maintenance of processors
13	.....Prepared backup processor (e.g., initializing cold backup) or updating backup processor (e.g., by checkpoint message)
14	....Of power supply
15	...State recovery (i.e., process or data file)
16	....Forward recovery (e.g., redoing committed action)
17	.....Reexecuting single instruction or bus cycle
18	....Transmission data record (e.g., for retransmission)
19	....Undo record
20	....Plural recovery data sets containing set interrelation data (e.g., time values or log record numbers)
21	....State validity check
22	....With power supply status monitoring
23	...Resetting processor
24	...Safe shutdown
25	..Fault locating (i.e., diagnosis or testing)
26	...Artificial intelligence (e.g., diagnostic expert system)
27	...Particular access structure
28	....Substituted emulative component (e.g., emulator microprocessor)
29	.....Memory emulator feature
30	....Built-in hardware for diagnosing or testing within-system component (e.g., microprocessor test mode circuit, scan path)
31	....Additional processor for in-system fault locating (e.g., distributed diagnosis program)
32	...Particular stimulus creation
33	....Derived from analysis (e.g., of a specification or by stimulation)
34	....Halt, clock, or interrupt signal (e.g., freezing, hardware breakpoint, single-stepping)
35	....Substituted or added instruction (e.g., code instrumenting, breakpoint instruction)
36	....Test sequence at power-up or initialization
37	...Analysis (e.g., of output, state, or design)
38	....Of computer software
39	....Monitor recognizes sequence of events (e.g., protocol or logic state analyzer)
40	...Component dependent technique
41	....For reliability enhancing component (e.g., testing backup spare, or fault injection)
42	....Memory or storage device component fault
43	....Bus, I/O channel, or network path component fault
44	....Peripheral device component fault
45	...Output recording (e.g., signature or trace)
46	...Operator interface for diagnosing or testing
47	..Performance monitoring for fault avoidance
48	..Error detection or notification

49	...State error (i.e., content of instruction, data, or message)		724	.Digital logic testing
50	....State out of sequence		725	..Programmable logic array (PLA) testing
51	.....Control flow state sequence monitored (e.g., watchdog processor for control-flow checking)		726	..Scan path testing (e.g., level sensitive scan design (LSSD))
			727	...Boundary scan
52	.....Error checking code		728	...Random pattern generation (includes pseudorandom pattern)
53	....Address error		729	...Plural scan paths
54	....Storage content error		730	...Addressing
55	...Timing error (e.g., watchdog timer time-out)		731	...Clock or synchronization
			732	..Signature analysis
56	....Bus or I/O channel device fault		733	..Built-in testing circuit (BILBO)
57	...Error forwarding and presentation (e.g., operator console, error display)		734	..Structural (in-circuit test)
			735	..Device response compared to input pattern
699	**PULSE OR DATA ERROR HANDLING**		736	..Device response compared to expected fault-free response
700	.Skew detection correction		737	..Device response compared to fault dictionary/truth table
701	.Data formatting to improve error detection correction capability		738	..Including test pattern generator
702	..Memory access (e.g., address permutation)		739	...Random pattern generation (includes pseudorandom pattern)
703	.Testing of error-check system		740	...Having analog signal
704	.Error count or rate		741	...Simulation
705	..Pseudo-error rate		742	...Testing specific device
706	..Up-down counter		743	...Addressing
707	..Synchronization control		744	...Clock or synchronization
708	..Shutdown or establishing system parameter (e.g., transmission rate)		745	..Determination of marginal operation limits
709	.Data pulse evaluation/bit decision		746	.Digital data error correction
710	.Replacement of memory spare location, portion, or segment		747	..Substitution of previous valid data
711	..Spare row or column		748	..Request for retransmission
712	.Transmission facility testing		749	...Retransmission if no ACK returned
713	..For channel having repeater		750	...Feedback to transmitter for comparison
714	..By tone signal		751	...Including forward error correction capability
715	..Test pattern with comparison		
716	...Loop-back		752	..Forward correction by block code
717	..Loop or ring configuration		
718	.Memory testing		753	...Double error correcting with single error correcting code
719	..Read-in with read-out and compare		754	...Error correction during refresh cycle
720	...Special test pattern (e.g., checkerboard, walking ones)		755	...Double encoding codes (e.g., product, concatenated)
721	..Electrical parameter (e.g., threshold voltage)		
722	..Performing arithmetic function on memory contents		
723	..Error mapping or logging		

756	....Cross-interleave Reed-Solomon code (CIRC)
757	...Parallel generation of check bits
758	...Error correcting code with additional error detection code (e.g., cyclic redundancy character, parity)
759	...Look-up table encoding or decoding
760	...Threshold decoding (e.g., majority logic)
761	...Random and burst error correction
762	...Burst error correction
763	...Memory access
764	....Error correct and restore
765	....Error pointer
766	....Check bits stored in separate area of memory
767	....Code word for plural n-bit (n>1) storage units (e.g., x4 DRAM's)
768	....Error correction code for memory address
769	....Dynamic data storage
770	.....Disk array
771	.....Tape
772	....Code word parallel access
773	....Solid state memory
774	...Adaptive error-correcting capability
775	...Synchronization
776	...For packet or frame multiplexed data
777	...Hamming code
778	...Nonbinary data (e.g., ternary)
779	...Variable length data
780	...Using symbol reliability information (e.g., soft decision)
781	...Code based on generator polynomial
782	....Bose-Chaudhuri-Hocquenghem code
783	....Golay code
784	....Reed-Solomon code
785	....Syndrome computed
786	..Forward error correction by tree code (e.g., convolutional)
787	...Random and burst errors
788	...Burst error
789	...Synchronization
790	...Puncturing

791	...Sequential decoder (e.g., Fano or stack algorithm)
792	...Trellis code
793	...Syndrome decodable (e.g., self orthogonal)
794	...Maximum likelihood
795	...Viterbi decoding
796	...Branch metric calculation
797	..Majority decision/voter circuit
798	.Error detection for synchronization control
799	.Error/fault detection technique
800	..Parity bit
801	...Parity generator or checker circuit detail
802	...Even and odd parity
803	...Parity prediction
804	...Plural dimension parity check
805	...Storage accessing (e.g., address parity check)
806	..Constant-ratio code (m/n)
807	..Check character
808	...Modulo-n residue check character
809	..Code constraint monitored
810	...Multilevel coding (n>2)
811	..Forbidden combination or improper condition
812	...Specified digital signal or pulse count
813	...Two key-down detector
814	...Data timing/clocking
815	...Time delay/interval monitored
816	...Two-rail logic
817	...Noise level
818	...Missing-bit/drop-out detection
819	..Comparison of data
820	...Plural parallel devices of channels
821	....Transmission facility
822	...Sequential repetition
823	....True and complement data
824	...Device output compared to input

FOREIGN ART COLLECTIONS

FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**

Any foreign patents or non-patent litera-
ture from subclasses that have been
reclassified have been transferred
directly to FOR Collection listed below.
These collections contain ONLY foreign
patents or nonpatent literature. The par-
enthetical references in the Collection
titles refer to the abolished subclasses
from which these Collections were derived.

        MEMORY TESTING (371/21.1)
        DIGITAL LOGIC TESTING (371/22.1)
        **DIGITAL DATA ERROR CORRECTION
          (371/30)**
FOR 100 .Scan path testing (LSSD) (371/
          22.3)
FOR 101 .Including test pattern generator
          (371/27)
FOR 102 .Block code (371/37.1)
FOR 103 ..Memory access (371/40.1)
FOR 104 .Convolutional code (371/43)
FOR 288 **ERROR/FAULT ANTICIPATION (371/4)**
        .Replacement with spare device or
          system (371/8.1)
FOR 289 ..Transmission facility or
          channel (371.8.2)
FOR 290 ..Memory (371/10.1)
FOR 291 ..Transmission facility (371/
          11.2)
FOR 292 ..Data processor or computer
          (371/11.3)
        DIAGNOSTIC TESTING (371/15.1)
FOR 293 .Programmable processor testing
          (371/16.1)
FOR 294 ..Emulator device (371/16.2)
FOR 295 ..Watchdog timer (e.g., time-out)
          (371/16.3)
FOR 296 ..Processor within diverse
          (microwave, photocopier) (371/
          16.4)
FOR 297 ..Error or fault, logging or
          tracking (371/16.5)
FOR 298 ..Dedicated maintenance subsystem
          (371/18)
FOR 299 .Testing of external device by
          programmable digital computer
          (371/20)
FOR 300 **ERROR DETECTION FOR
        SYNCHRONIZATION CONTROL (371/
        47.1)**